ISO9001:2008 Certified SCI Quality System

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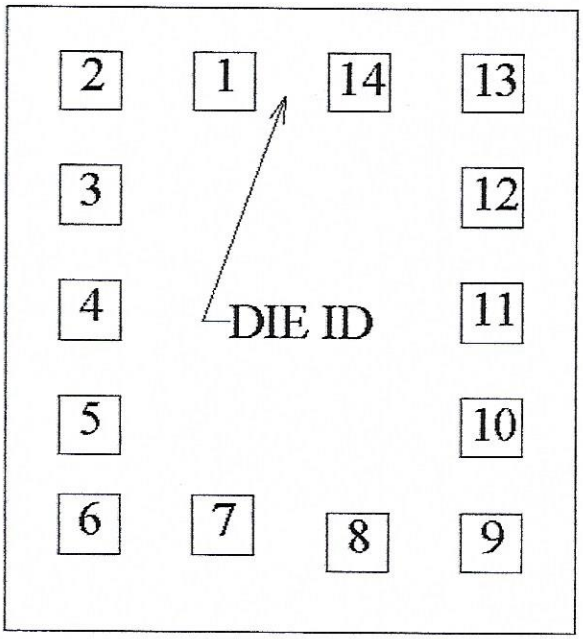
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.



PAD	FUNCTION
1	COLLECTOR Q1
2	BASE Q1
3	EMITTERS Q1 & Q2
4	BASE Q2
5	COLLECTOR Q2
6	BASE Q3
7	EMITTER Q3
8	COLLECTOR Q3
9	BASE Q4
10	EMITTER Q4
11	COLLECTOR Q4
12	BASE Q5
13	EMITTER Q5 & SUBSTRATE
14	COLLECTOR Q5

APPLICATION NOTE:

SUBSTRATE MUST BE CONNECTED TO THE MOST NEGATIVE POINT IN THE EXTERNAL CIRCUIT TO MAINTAIN ISOLATION BETWEEN TRANSISTORS AND TO PROVIDE FOR NORMAL TRANSISTOR ACTION.

NOTE:

Top Material: Aluminum
Backside Material: Silicon
Bond Pad Size: .004" X .004" min.
Backside Potential: See Note
Mask Ref: 0235

APPROVED BY: DK	**DIE SIZE .034 x .038"**	**DATE: 9/22/16**
MFG: National Semi.	**THICKNESS .025"**	**P/N: CA3045**